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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
CHOI, WOO H

ART UNIT	PAPER NUMBER
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,003	KIRSCH, GRAHAM	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11-15,18019,22-29,33-37,and 41-51* is/are rejected.

7)☒ Claim(s) *9,10,16,17,20,21,30,31,38 and 39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2. The drawings are objected to because figure 5 does not clearly show the connections between the output of the tri-state driver and the individual bus lines. The drawing shows the 8 bus lines as a single line while the outputs of each of the tri-state devices are connected to only on of the 8 bus lines, according to the specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 8, 11 – 15, 22 – 29, 33 – 37, and 41 – 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Fung (US Patent No. 4,380,046.)

5. With respect to claims 1 and 2, Fung discloses an active memory device comprising:

a main memory (claim 7);

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection (col. 5 lines 50 – 56); and

a circuit coupled between said main memory and said plurality of processing elements (figure 2), said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements (abstract and figure 4.) The circuit is further adapted to write data from said plurality of processing elements to said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (abstract and figure 4.)

6. With respect to claims 3 and 4, Fung discloses that a plurality of processing elements in a first group are coupled to a plurality of data buses of main memory (figure 4, D1 – D10), each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory (figure 4, "(i, j)", also figure 9, LMU effective address associated with each element) wherein the first group includes eight processing elements (figure 4, shows 9 elements, hence includes 8 elements.)

7. With respect to claim 5, the circuit further comprises:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data

between its associated respective one of said plurality of processing elements and said main memory (figure 2, 56 and figure 5, logic slider sub unit connects the processing elements and the main memory)

8. With respect to claim 6, the circuit further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory (figure 5); and

a first multiplexer (94) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements.

9. With respect to claims 7 and 8, the logic circuit further comprises:

a second multiplexer (80) having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit (76);

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses (78); and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second

multiplexer (the unnumbered tri-state device in figure 5 that is directly coupled to the input of one of the AND gates, it is coupled to the register, data bus and the multiplexer via other gates and circuits.) The output of said second tri-state device is coupled to said respective one of said plurality of data buses via other gates and logic circuits.

10. With respect to claim 11 and 12, Fung discloses a memory device comprising:

a main memory (claim 7);

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit and a single bit data input; and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements (figure 5),

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time (abstract, figure 4.) The data path circuit is further adapted to write data from said plurality

of processing elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (abstract and figure 4.)

11. With respect to claim 13, each of said plurality of data path circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit (figure 5); and

a first multiplexer (94) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to said output of said data path circuit.

12. With respect to claim 14 and 15, each of said plurality of logic circuits further comprises:

a second multiplexer (80) having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit (76);

a first tri-state device having an input: coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses (78); and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer (the unnumbered tri-state device in figure 5 that is directly coupled to the input of one of the AND

gates, it is coupled to the register, data bus and the multiplexer via other gates and circuits.) The output of said second tri-state device is coupled to said respective one of said plurality of data buses via other gates and logic circuits.

13. With respect to claim 18, Fung discloses a circuit for connecting a memory device and a processing element of an active memory comprising:

a first multiplexer (80) having a first input coupled to said processing element and a second input coupled to a data bus of said memory device;

a first register having an input and an output, said input being coupled to an output of said first multiplexer (76);

a second multiplexer having an input coupled to said output of said first register and an output coupled to said processing element (94, input coupled registers of other elements and its own element through other elements, see figure 4);

a first tri-state device having an input coupled to said output of said first register and an output coupled to said data bus (78); and

a second tri-state device having an input coupled to said output of said first register and an output coupled to said data bus and a third input of said first multiplexer (the unnumbered tri-state device in figure 5 that is directly coupled to the input of one of the AND gates, it is coupled to the register, data bus and a third input of the first multiplexer via other gates and circuits.) The output of said second tri-state device is coupled to the data bus via other gates and logic circuits

14. With respect to claim 19, the output of said second tri-sate device is coupled to a different data bus than said output of said first tri-state device (see figure 5, first tri-state device is coupled to 52 and the second tri-state device is coupled to 98.)

15. With respect to claim 22 and 23, Fung discloses a processing system (figure 1) comprising:

a processing unit (figure 1, 22); and

an active memory device coupled to said processing unit, said active memory device comprising:

a main memory (claim 7);

a plurality of processing elements, each of said plurality of processing elements being coupled to a respective portion of said main memory by a single bit connection (col. 5, lines 50 – 56); and

a circuit coupled between said main memory and said plurality of processing elements (figure 2), said circuit writing data from said plurality of processing elements to said memory in a horizontal mode and reading data stored in said main memory in a horizontal mode from said main memory to said plurality of processing elements (abstract and figure 4.) The circuit is further adapted to write data from said plurality of processing elements to said memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (abstract and figure 4.)

16. With respect to claims 24 and 25, a plurality of processing elements in a first group are coupled to a plurality of data buses of said main memory (figure 4, D1 – D10), each of said plurality of data buses being associated with a respective one of a plurality of addresses in said main memory (figure 4, "(i, j)", also figure 9, LMU effective address associated with each element), wherein the first group includes eight processing elements (figure 4, shows 9 elements, hence includes 8 elements.)

17. With respect to claim 26, the circuit further comprises:

a plurality of circuits, each of said plurality of circuits being associated with a respective one of said plurality of processing elements, each of said plurality of circuits passing data between its associated respective one of said plurality of processing elements and said main memory (figure 2, 56 and figure 5, logic slider sub unit connects the processing elements and the main memory)

18. With respect to claim 27, each of the plurality of circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to a respective one of a plurality of data buses, each of said plurality of data buses being coupled to said main memory (figure 5); and

a first multiplexer (94) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to its associated respective one of said plurality of processing elements.

19. With respect to claims 28 and 29, each of the plurality of logic circuits further comprises:

a second multiplexer (80) having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit (76);

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses (78); and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer (the unnumbered tri-state device in figure 5 that is directly coupled to the input of one of the AND gates, it is coupled to the register, data bus and the multiplexer via other gates and circuits.) The output of said second tri-state device is coupled to said respective one of said plurality of data buses via other gates and logic circuits.

20. With respect to claim 32, the processing unit and said active memory device are on a same chip (col. 5, lines 39 – 44.)

21. With respect to claims 33 and 34, Fung discloses a processing system comprising:

a processing unit (figure 1, 22); and

a memory device coupled to said processing unit, said memory device comprising:

a main memory (claim 7);

a plurality of processing elements, each of said plurality of processing elements being associated with a respective portion of said main memory, each of said plurality of processing elements having a single bit data output and a single bit data input (col. 5, lines 50 – 56); and

a plurality of data path circuits, each of said plurality of data circuits being coupled between said main memory and one of said plurality of processing elements, each of said plurality of data path circuits having a plurality of inputs, a first input of said plurality of inputs being coupled to said single bit output of a respective one of said plurality of processing elements, at least a second input of said plurality of inputs being coupled to a respective one of a plurality of data buses of said main memory, and an output coupled to said single bit input of a respective one of said plurality of processing elements (figure 5),

wherein each of said data path circuits is adapted to receive data from said respective one of said plurality of processing elements a single bit at a time and write said data to said main memory in a horizontal mode, and to receive data stored in said main memory in a horizontal mode and output said data to said respective one of said plurality of processing elements a single bit at a time (abstract and figure 4.) Each of the data path circuit is further adapted to write data from said plurality of processing elements to said main memory in a vertical mode and read data stored in said main memory in a vertical mode from said main memory to said plurality of processing elements (abstract and figure 4.)

22. With respect to claim 35, each of said plurality of data path circuits further comprises:

a plurality of logic circuits, each of said plurality of logic circuits having a first input and an output, said first input being coupled to said at least a second input of said plurality of inputs of said data path circuit (figure 5); and

a first multiplexer (94) having a plurality of inputs, each of said plurality of inputs being coupled to an output of a respective one of said plurality of logic circuits, and an output coupled to said output of said data path circuit.

23. With respect to claims 36 and 37, each of said plurality of logic circuits further comprises:

a second rnultiplexer (80) having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output coupled to said output of said logic circuit (76);

a first tri-state device having an input coupled to said output of said first register and an output coupled to said respective one of said plurality of data buses (78); and

a second tri-state device having an input coupled to said output of said first register and an output coupled to one of said plurality of data buses and a third input of said second multiplexer (the unnumbered tri-state device in figure 5 that is directly coupled to the input of one of the AND gates, it is coupled to the register, data bus and the multiplexer via other gates and circuits.) The output of said second tri-state device is coupled to said respective one of said plurality of data buses via other gates and logic circuits.

24. With respect to claim 40, the processing unit and said active memory device are on a same chip (col. 5, lines 39 – 44.)

25. With respect to claim 41, Fung discloses a method for writing data from a processing element to a memory device comprising the steps of:

providing a plurality of data bits in a serial manner from said processing element to a data circuit;

passing said data through said data circuit; and

writing said data to said memory device, wherein said data circuit passes said data directly to said memory device in a horizontal mode (abstract, and claim 7.)

26. With respect to claim 42, the step of passing the data further comprises:

outoutputting each bit of said plurality of data bits from said data circuit on a different data bus (figure 5, 98) associated with said memory device; and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to a location in said memory device associated with a different address (figure 5, 98, and figure 4, a bit written onto 98 gets copied to the neighboring PEs)

27. With respect to claim 43, the step of outputting further comprises:

passing each bit of said plurality of data bits through a respective register (figure 5, 76).

28. With respect to claim 44, each different memory address has an associated plurality of bits (figure 2, 50 and 54), and wherein said step of writing each said data bit further comprises:

writing said each bit into a same bit of said associated plurality of bits in each said different memory address (abstract and claim 7, as data bits get written, or shifted to neighboring elements, each bit get written into a same bit in different memory address.)

29. With respect to claim 45, the circuit is further adapted to pass at least a portion of said data to said memory device in a vertical mode (abstract.)

30. With respect to claim 46 the step of passing said at least a portion of said data further comprises:

outputting each bit of said plurality of data bits from said data circuit on a different data line of a single data bus associated with said memory device (figure 5, 98); and

wherein said step of writing said data further comprises writing said each bit of said plurality of bits data bits to successive bit locations associated with a single address (figure 2, 54, and claim 3, BC/SR stores bits in successive locations.)

31. With respect to claim 47 the step outputting further comprises:

passing each bit of said plurality of data bits through a respective register (figure 2, 54, also see figure 6.)

30. With respect to claim 48, Fung discloses a method for reading data stored in a memory device and providing said data to a processing element, said method comprising the steps of:

providing a plurality of data bits from said memory device to a data circuit;

passing said data through said data circuit; and

outputting said data to said processing element in a serial manner (claim 7),

wherein said data is stored in said memory device in a horizontal mode (abstract.)

31. With respect to claim 49, the step of passing said data further comprises:

passing each bit of data associated with a single address through a respective register (figure 2, 76); and

inputting said each bit of data associated with said single address to a multiplexer (80),

wherein said multiplexer outputs said each bit of data in a serial manner to said processing element (claim 7.)

32. With respect to claim 50, at least a portion of said data is stored in said memory device in a vertical mode (abstract.)

33. With respect to claim 51, the step of passing said at least a portion of said data further comprises:

passing a respective bit of data associated with a different address through a respective register (figure 4, and figure 5, 76); and

inputting each said respective bit of data associated with said different address to a multiplexer (94),

wherein said multiplexer outputs said each said respective bit of data in a serial manner to said processing element (figure 5, 94, the multiplexer outputs bit of data to the processing element through coupling circuits.)

Allowable Subject Matter

34. Claims 9 – 10, 16 – 17, 20 – 21, 30 – 31, and 38 – 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

35. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach or suggest the following:

[Claims 9 and 10] The active memory device according to claim 6, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

[Claims 16 and 17] The memory device according to claim 13, wherein each of said plurality of logic circuits further comprises:

a second Multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second Multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

[Claims 20 and 21] The circuit according to claim 18, further comprising:

a second register having an input coupled to said output of said first multiplexer;

a third multiplexer having a first input, a second input, and an output, said first input being connected to an output of said second register, said output from said first register being coupled to said second input, said output being coupled to said input of said second multiplexer; and

a fourth multiplexer having a first input, a second input, and an output, said first input being coupled to said output of said first register, said second input being coupled to said output of said second register, said output being coupled to said input of said first and second tri-state devices.

[Claims 30 and 31] The processing system according to claim 27, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said associated respective one of said plurality of processing elements and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

[Claims 38 and 39] The processing system according to claim 35, wherein each of said plurality of logic circuits further comprises:

a second multiplexer having a first input coupled to said first input of said data path circuit and a second input coupled to said input of said logic circuit;

a first register having an input coupled to an output of said second multiplexer and an output;

a second register having an input coupled to said output of said second multiplexer and an output;

a third multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output coupled to said output of said logic circuit;

a fourth multiplexer having a first input coupled to said output of said first register, a second input coupled to said output of said second register, and an output;

a first tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to said respective one of said plurality of data buses; and

a second tri-state device having an input coupled to said output of said fourth multiplexer and an output coupled to one of said plurality of data buses and a third input of said second multiplexer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

whc
August 5, 2002

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100